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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,728	01/24/2001	Bassel Beidas	PD-200213	1225

7590 08/16/2004

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EXAMINER
MURPHY, RHONDA L

ART UNIT	PAPER NUMBER
2667	

DATE MAILED: 08/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/768,728	BEIDAS ET AL.	
	Examiner	Art Unit	
	Rhonda L Murphy	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-4, 6-9,13-15,17,18,20 is/are rejected.

7)☒ Claim(s) 5,10-12,16,19 and 21 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 24 January 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because the AGC Block Diagram of Figure 11 is shown as item "112". According to the specification, Figure 11 should be designated as item "116". Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities and shall be changed as follows: AGC block "112" changed to "116" in paragraph 54 of page 13;

mode switch "42" changed to "142" of same paragraph; 128 FFT block "130" changed to "230" in the last two sentences of paragraph 61 and second sentence of paragraph 62 on page 16; "VCR" to "VCO" in paragraph 66; and beacon demodulator "110" in paragraph 68 should be denoted as "112".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Fenton et al. (US 5,809,064).

Regarding claim 1, Fenton teaches a method of receiving an input signal at a receiver (col. 4, lines 29-31); sampling said signal at a clock rate to generate signal samples (col. 4, lines 39-42); providing said signal samples to said delay lock loop circuit (col. 3, lines 20-24); controlling said delay lock loop circuit to provide an output representing a phase delay of the received signal (col. 3, lines 20-26); adjusting the clock rate based on said phase delay (col. 3, lines 24-26); and determining said frequency at which said terminal transmits said transmission signal based on said phase delay (col. 4, lines 63-66).

Regarding claim 2, Fenton teaches a method wherein the input signal comprises synchronization information in discontinuous time slots (col. 4, lines 39-41).

Regarding claim 13, Fenton teaches a receiver for receiving a signal (col. 4, lines 29-31), a local signal generator for generating an early local signal and a late local signal at a local frequency (col. 6, lines 42-44), said early local signal being substantially similar to said synchronization information offset forward in time (col. 9, lines 24-30), said late local signal being substantially similar to said synchronization information offset backward in time (col. 9, lines 20-23), a discriminator for correlating said signal against said early local signal and for correlating said signal against said late local signal (col. 11, lines 61-63), and for generating a discriminator output representative of the difference between the two correlations (col. 11, lines 64-66), and a delay lock loop circuit for receiving said discriminator output (col. 12, lines 1-2), wherein said delay lock loop circuit generates an output which is used to adjust said local frequency (col. 12, lines 25-30).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fenton et al. (US 5,809,064) in view of Johnson (US 5,414,741).

Regarding claims 3 and 14, Fenton teaches the method as set forth in the rejection of claims 1 and 13 as described above.

Fenton fails to teach a delay lock loop circuit comprising at least a third order tracking loop.

However, Johnson teaches a phase lock loop circuit comprising at least a third order tracking loop (col. 8, lines 66-68; col. 9, lines 1-2).

In view of this, having the teaching of Fenton and then given the teaching of Johnson, it would have been obvious to one having ordinary skill in the art at the time the invention was made, to modify the system of Fenton to incorporate at least a third order tracking loop, so as to provide better dynamic tracking of receiver input signals (col. 13, lines 10-11).

7. Claims 4,6-9,15,17,18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fenton et al. (US 5,809,064) in view of Krasner (US 6,633,255). **Regarding claims 4, 6, 15 and 17**, Fenton teaches the method as set forth in the rejection of claim 1,13 and 14 as described above.

Fenton fails to teach the following limitations taught by Johnson: a delay lock loop circuit further comprising a low order gain loop (**second order loop**); and said delay lock loop circuit initially using a low order gain loop (**acquired lock as a second order loop**) and subsequently using at least third order tracking loop (**then converted to third order loop operation**) to provide an output (col. 20, lines 14-17).

In view of this, having the teaching of Fenton and then given the teaching of Johnson, it would have been obvious to one having ordinary skill in the art at the time the invention was made, to modify the system of Fenton to utilize both low order gain

loop and third order tracking loop, so as to receive the benefits of both loops and provide a higher quality output signal.

Regarding claims 7 and 18, Fenton teaches a method of a sampling circuit adapted to sample the incoming communication signal at a sampling rate and for producing a series of samples at the sampling rate (col. 4, lines 39-42) and a lock detector adapted to determine whether the satellite terminal is locked onto the incoming signal based on the output (col. 10, lines 57—67; col. 11, lines 1-4).

Fenton does not teach the following limitations taught by Krasner: a method of generating local phase signals substantially identical to the series of phase signals in the incoming signal (col. 9, lines 45-49); a fast Fourier transform (FFT) circuit adapted to receive a combination signal representing a combination of the samples and the local phase signals (see Fig.10 and Fig. 11; col. 11, lines 1-7), and FFT circuit generating an output based on said combination signal (Fig. 11).

In view of this, having the teachings of Fenton and then given the teaching of Krasner, it would have been obvious to one having ordinary skill in the art at the time the invention was made, to modify the system of Fenton to incorporate the local phase signals and FFT circuit of Krasner, so as to determine whether the satellite terminal is locked onto the incoming signal based on the output of the FFT circuit and provide more efficient processing.

Regarding claims 8 and 20, Fenton teaches the method as set forth in the rejection of claims 7 and 18 as described above.

Fenton fails to teach local phase signals comprising a series of digital values.

However, Krasner teaches local phase signals comprising a series of digital values (col. 9, lines 59-61).

In view of this, having the teaching of Fenton and then given the teaching of Krasner, it would have been obvious to one having ordinary skill in the art at the time the invention was made, to modify the system of Fenton to incorporate local phase signals comprising digital values, so as to facilitate signal processing.

Regarding claim 9, Fenton teaches an incoming signal comprising a series of digital samples generated at a sampling rate (col. 3, lines 11-13).

Allowable Subject Matter

8. Claims 5, 10-12, 16, 19 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art does not teach:

Regarding claim 5, determining a difference between said frequency and an expected frequency; and wherein the step of controlling the delay lock loop further comprises using a low order gain loop until the difference is less than a threshold value, and subsequently using the at least third order loop.

Regarding claim 10, determining an offset between the frequency of the incoming signal and the sampling rate based on the output of the FFT circuit, and adjusting the sampling rate based on the offset.

Regarding claim 11, multiplying an incoming signal and a local phase signals to generate a product signal.

Regarding claim 12, decimating a product signal to create a combination signal.

Regarding claim 16, a frequency offset determining circuit adapted to determine a difference between the frequency of the signal and an expected frequency; and wherein the delay lock loop circuit uses simple gain loop until the difference is less than a threshold value.

Regarding claim 19, an offset estimator adapted to determining an offset between the frequency of the incoming communication signal and the sampling rate based on the output of the FFT circuit, and to adjust the sampling rate based on the offset.

Regarding claim 21, a decimator adapted to decimate a combination signal before a combination signal is received by the FFT circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rhonda L Murphy whose telephone number is (703) 308-9557. The examiner can normally be reached on Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (703) 305-4798. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KWANG BIN YAO
PRIMARY EXAMINER

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